REMARKS

Claims 27 and 35-38 were previously canceled. Claims 39-46 have been added. Claims 25, 26, 28-34, and 39-46 are pending in this application.

Claims 25 and 28-34 stand rejected under 35 USC § 102(e) as being anticipated by Heo, U.S. Patent No. 6.389,689 ("Heo"). Applicants respectfully traverse this rejection and request reconsideration.

Heo does not disclose all limitations of independent claim 25. Specifically, Heo fails to disclose a metal layer having "a stiffness sufficient to enable simultaneous dicing of said semiconductor devices edges, said substrate edges, and said metal layer edges, so as to provide said package with aligned edges," as recited by independent claim 25. The Office Action asserts that "the phrase 'simultaneous dicing of said semiconductor device edges, said dielectric substrate edges, and metal layer edges' is product-by-process language." (Office Action at 3). Applicants, however, submit that in the context of claim 25 this language defines a structure having distinct and defined characteristics.

The Federal Circuit has held that claim limitations which confer distinct and defined characteristics of a structure are "pure product claims" and not product-by-process claims. In Hazani v. U.S. Int'l Trade Comm'n, the Federal Circuit considered patent claims to a memory cell comprising a conductive plate having a surface that was "chemically engraved." Hazani v. U.S. Int'l Trade Comm'n, 126 F.3d 1473, 44 USPQ2d 1358 (Fed. Cir. 1997). The Federal Circuit said that the claims were "best characterized as pure product claims, since the 'chemically engraved' limitation, read in context, describes the product more by its structure than by the process used to obtain it." Id.

Similarly, in the present claims, the language "simultaneous dicing of said semiconductor device edges, said dielectric substrate edges, and metal layer edges" describes the semiconductor package more by its structure than by the process used to obtain it. In the context of claim 25, the language defines the stiffness of the metal layer to be a stiffness "sufficient to enable simultaneous dicing of said semiconductor devices edges, said substrate edges, and said metal layer edges, so as to provide said package with aligned edges." Additionally, in the context of claim 25, this language defines the alignment of the edges of the semiconductor package. Because the semiconductor devices, substrate, and metal layer are diced simultaneously, the edges of the semiconductor package are aligned to such a degree as provided when these structures are diced simultaneously. Accordingly, this language defines the structural characteristics of the semiconductor package, and specifically the structural characteristics of the metal layer and package edges. In view of Hazani, the limitation of claim 25 can only be a structural limitation and not a product-by-process limitation.

Even assuming that the limitations of claim 25 are product-by-process limitations, "[t]he structure implied by the process steps should be considered when assessing the patentability of product-by-process claims over the prior art." This is especially the case where "the product can only be defined by the process steps by which the product is made, or where the manufacturing process steps would be expected to impart distinctive structural characteristics to the final product." MPEP § 2113 (citing In re Garnero, 412 F.2d 276, 279, 162 USPQ 221, 223 (CCPA 1979)). Therefore, the language cited by the Office Action should be considered in the context of claim 25 as it relates to the stiffness of the metal layer and the alignment of the semiconductor package edges.

The Office Action also states that Heo discloses a metal layer that "has a stiffness sufficient to enable simultaneous dicing of said semiconductor device edges, said dielectric substrate edges, and said metal layer edges, so as to provide said package with aligned edges." (Office Action at 3). Applicants respectfully submit that Heo does not provide such a disclosure. Although Heo discloses a copper layer 21 (FIG. 6), Heo is silent about the particular stiffness, if any, of the copper layer 21. Additionally, Heo discloses that the circuit board sheet containing the metal layer 21 and the semiconductor chip are diced at different times. Therefore, Heo is not concerned with the metal layer 21 having a stiffness sufficient to enable simultaneous dicing of the semiconductor chip and the metal layer, as in the present invention.

For at least these reasons, withdrawal of the rejection of claims 25 and 28-34 is respectfully requested. Claim 26 depends from independent claim 25 and is believed to be allowable along with claim 25 and for other reasons. Favorable action on the application, as amended, with claims 25, 26, 28-34, and 39-46, is solicited.

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Respectfully submitted,

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